A

Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P3373 Total Pages 4

First Named Inventor or Application Identifier James Akiyama

Express Mail Label No. EL 03416 3396 US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form, in duplicate
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 16, including cover)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 9)

4. X Oath or Declaration (Total Pages 4)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __X__ Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: _____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _

18. **Correspondence Address**
_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)
or
__X__ Correspondence Address Below

NAME James H. Salter (Reg. No. 35,668)
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
ADDRESS 12400 Wilshire Boulevard
Seventh Floor
CITY Los Angeles STATE California ZIP CODE 90025-1026
Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PTO/SB/17(10/96)
Approved for use through 09/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT ($) 830.00

Complete if Known:

Application No.	Unassigned
Filing Date	October 1, 1998
First Named Inventor	James Akiyama
Group Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket No.	42390.P3373

METHOD OF PAYMENT (check one)

1. [ ] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number _____
   Deposit Account Name _____

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 and credit any over payments to Deposit Account Number 02-2666**

   [ ] **Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.131(b)**

2. X **Payment Enclosed**
   X **Check**
   _____ **Money Order**
   _____ **Other**

FEE CALCULATION (fees effective 10/01/97)

1. **FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility application filing fee	790.00
106	330	206	165	Design application filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $_____

2. **CLAIMS**

			Extra		Fee from below		Fee Paid
Total Claims	4	- 20 =	0	X	0	=	0
Independent Claims	2	- 3 =	0	X	0	=	0
Multiple Dependent Claims			0	X	0	=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
103	22	203	11	Claims in excess of twenty	
102	82	202	41	Independent claims in excess of 3	
104	270	204	135	Multiple dependent claim	
109	82	209	41	Reissue independent claims over original patent	
110	22	210	11	Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) $ 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
128	2,060	228	1,030	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	790	246	395	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (see 37 CFR 1.129(a))	

SUBTOTAL (3) $ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: James H. Salter

Signature _____ Date 10/1/98

Reg. Number 35,668 Deposit Account User ID _____ (complete if applicable)

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number: EL 03416 3396 US

Date of Deposit: October 1, 1998

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to BOX APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

Barbara Skliba

Name of Person Mailing Paper or Fee

Barbara Skliba

Signature of Person Mailing Paper or Fee

10/1/98

Date Signed

42390.P3373

PATENT

UNITED STATES PATENT APPLICATION

for

VIRTUALIZED STRIPING CONTROLLER

Applicant:

James Akiyama

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026
(408) 720-8598

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number EL 03416 3396 US

Date of Deposit October 1, 1998

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to BOX APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

Barbara Skliba
Typed or printed name of person mailing paper or fee

Barbara Skliba 10/1/98
Signature of person mailing paper or fee Date

VIRTUALIZED STRIPING CONTROLLER

FIELD OF THE INVENTION

The invention is generally directed at a low cost approach to gaining higher performance from disk drives by striping.

DESCRIPTION OF THE PRIOR ART

Parallel transfer drives were the first effort at gaining hard disk performance by making parallel accesses. In a parallel transfer drive, data is written and read simultaneously off of multiple platters in a single housing. But parallel transfer drives, while fast, are very expensive.

The concept of striping was developed to achieve the advantages of parallel transfer drives at a much lower cost by combining two totally separate, low-cost drives with sophisticated software. Striping creates a single virtual disk from two physical drives. The sectors of the two physical disks are interleaved on the virtual drive. The effect is that the virtual disk has double the capacity of a single disk and double the data transfer rate of a single disk drive since the two physical drives can be read and written in parallel.

Figure 1 is a schematic that illustrates the basic concept of striping. Referring now to Figure 1, a virtual drive 3 is a model of the striped physical drives 4 and 5. Physical drives 4 and 5 are separate disk drives each having its own set of drive electronics 6 power supplies and

mirrors (not shown) and disks which in this example are single disks 7a and 7b. Each disk is divided into tracks and each track is divided into sectors. For purposes of illustration, each disk is shown as having 8 sectors (numbered 0-7). Sectors 0-7 on physical drive 4 correspond to sectors 40 - 47 on virtual disk 3. And sectors 0 - 7 on physical drive 5 correspond to sectors 50-57 on virtual disk drive 3. Striping creates a new interface which is indicated at reference numeral 2 in Fig. 1.

Striping was first introduced in SCSI (Small Computer System Interface) drives for work stations. The original motivation for striping was to gain more performance in the work station environment where performance was previously limited to a data transfer rate of 10 megabits per second that was mandated by a drive rotating at 3600 rpm and having 17 sectors of 512 bytes per track.

Later, the basic striping technology developed for SCSI drives was applied to the integrated drive electronics ("IDE") drive. This transition was motivated by the even lower cost and wider adoption of the IDE drive in the Industry Standard Architecture ("ISA") based computer (IBM compatible) market. But these drives still used the architecture developed in the SCSI interface environment to implement the striping IDE drive which relies on a dedicated microprocessor.

These IDE controllers stripe the data by simultaneously reading data from the primary and secondary IDE channels. Software drivers are then used to encode and decode the striped data streams. In this approach, there is a maximum of four physical disk drives and two logical

drives per IDE interface. Each logical disk drive is mapped to two physical disk drives through a sophisticated software driver.

An IDE hard disk drive integrates both a hard disk drive and its controller in one unit - inside the drive housing. An IDE drive appears to the host computer as two blocks of I/O (input/output) registers, a command register block and a control register block, with addresses in the I/O space of the ISA bus. The IDE drive interfaces to an ISA or PCI (Peripheral Component Interconnect) bus. The interface between an IDE drive and the system bus, sometimes called a host adapter, is typically a small card that plugs into the ISA bus. On the IDE side of the card, a 40 pin ribbon cable leads to the remainder of the IDE electronics. The IDE interface essentially reduces the width of the ISA bus by eliminating the ISA address lines and substituting two commands, CS1FX and CS3FX, which select respectively the command register block or the control register block from an ISA bus address. Parallel data is supplied to the IDE interface where it is converted to serial data, converted to analog and written on the media in specified locations called addresses. IDE electronics detect errors through the addition of error detection algorithms added to each sector. But the IDE electronics typically do not correct errors. Rather, the IDE drive passes raw error data back to the host for correction.

The IDE specification limits the sector per track to 64; the tracks to 2048 per disk, 16 heads per disk and 2 drives per interface. A PC (Personal Computer) type computer system can have two IDE interfaces. That is, two channels are located at two different addresses in I/O space. In a standard computer using an IDE interface, this means that it is possible to hook up a maximum of four physical drives conventionally.

The problem with the prior art approaches is that the standard IDE software drivers cannot be used, and special device drivers must be written for each operating system. In addition, the hardware is expensive since an additional microprocessor is required.

SUMMARY OF THE INVENTION

The present invention is a striping disk controller used in a computer system that includes a CPU connected to a system bus and running an operating system and having a BIOS. A disk drive interface is connected to the system bus and communicates with the BIOS. First and second disk drives are provided, each including analog electronics, data separator electronics, formatting electronics and head positioning electronics. A striping controller is connected between the first and second disk drives and the interface. The striping controller causes data being communicated between the system bus and the first and second drives to be written and read to and from the first and second dries substantially in parallel, alternating sectors on each drive. Striping increases data transfer rates by accessing two drives simultaneously. During read and write operations, both drives are accessed simultaneously which has the effect of doubling the effective transfer rate and capacity.

BRIEF DESCRIPTION OF THE DRAWING

The preferred embodiment will be described in connection with the Drawing in which:

Figure 1 is a schematic of a virtual disk.

Figure 2 is a process flow chart showing how disk accesses are made in a conventional IDE system.

Figure 3 is a schematic of the data structure of a system request for access to an IDE drive.

Figure 4 is a block diagram of a prior art striping system.

Figure 5 is a high-level block diagram of the present invention as applied to two virtual disk drives, and four physical drives.

Figure 6 is a schematic of the system request data structure broken out into its component parts and showing how bits are shifted according to the invention.

Figure 7 is an illustration of an example of how the mapping set out in Figure 6 effects striping.

Figure 8 is a schematic of a preferred embodiment of a striping controller according to the present invention.

Figure 9 is a table indicating how virtual sector starting addresses and sector counts are mapped to physical starting address and counts.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is a striping disk controller used in a computer system that includes a CPU connected to a system bus and running an operating system and having a BIOS (Basic Input/Output System). In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other circumstances, well-known structures and devices, and interfaces are shown in block diagram form in order to avoid unnecessarily obscuring the present invention.

Figure 2 is a process flow chart showing how disk accesses are made in a conventional IDE system. In process block 20 a requirement for X bytes of storage is generated by an application. The application passes this request to the operating system 22. Operating system 22 translates the application request to a file system request. In the case of conventional DOS (Disk Operating System), the file system request includes an identity of "virtual sectors", which are incremented corresponding to the disk track and head. That is, the zero sector of track 2 is one virtual sector higher than the last physical sector on track 1. A Basic Input/Output Operating System (BIOS) is a set of machine language routines, usually found in a ROM (read only memory) on the mother board, that work with I/O interfaces at the lowest level and thereby relieve higher level code of this task. In the case of disk storage, the BIOS translates virtual sector requests received from the operating system into the physical IDE requests at process step 24. Physical IDE request means a request for a specific sector, a specific track, a specific head

and a specific drive. The physical request is made in compliance with the IDE specification and supplied to IDE interface 26 which decides the drive request and passes on the sector, track and head requests either over bus 28 to IDE drive 30 or over bus 32 to IDE drive 34. Each IDE drive contains conventional IDE electronics 36 and a disk assembly 38 of one or more disks up to 16 surfaces. IDE electronics 36 performs several functions: It translates a request for access request supplied from the BIOS to specific physical sectors, tracks and heads on disk 38. It also performs data separation which on reads generates a clock and digital data signal in serial format. It also performs formatting functions, namely serial to parallel conversion on reads and parallel to serial on writes. It also performs head positioning and analog data functions.

Figure 3 is a schematic of the data structure of a system request for access to an IDE drive that is relevant to the present invention. It is generally that portion which relates to a particular disk and the location on that disk that specific data is to be written or read. Referring now to Figure 3, a system access request structure 40 consists of a sector request bit string 42 of 6 bits that can uniquely identify 64 sectors; a track request bit string 44 of 11 bits that can uniquely identify 2048 tracks; a head request bit string of 4 bits that can uniquely identify 16 heads and a drive bit 48 that can identify 2 drives. Enhanced IDE (EIDE) will increase the allowable tracks. It will be apparent to those of ordinary skill in the art that equivalent variations of basic IDE may be implemented without departing from the scope of the present invention.

Figure 4 is a block diagram of a prior art striping system. Referring to Figure 4, the two IDE interfaces 50 and 52 are connected via busses 54 and 56 to striping controller 58. A microprocessor 60 is connected by bus 62 to striping controller 58. Microprocessor 60 runs the code that determines the type of striping action - e.g. interleaving the two disk drives to get better performance or mirroring for better redundancy. Buffer memory 64 stores some of the code for microprocessor 60 and acts as a cache for microprocessor 60. Microprocessor 60 is also interfaced to a host computer system across bus 66 such as ISA or PCI bus. The IDE electronics returns status and error signals to microprocessor 60. Microprocessor 60 performs error correction and returns status and error messages to the host. Thus, part of the function of microprocessor 60 is to manage the status and error signals from two different physical disk drives and report only one status and error to the host. The host believes that there is only one hard disk drive with twice the performance and twice the capacity, while in fact there are two disk drives that are interleaved.

The output from striping controller 58 on busses 54 and 56 are compliant to the IDE specification since they connect to IDE interfaces 50 and 52. Striping logic 58 performs the functions of translating the microprocessor 60 requests into the two physical IDE buses.

In this implementation, the disk drive does not look like an IDE drive to the host. Rather a disk access looks like a host to host communication. From an operating system perspective, this means that the standard IDE software driver cannot be used.

Figure 5 is a high-level block diagram of the present invention as applied to a single IDE

interface. Referring now to Figure 5, system bus 66 is connected to IDE interface 26. System bus 66 may be an ISA or PCI bus, for example. IDE Bus 28 connects IDE interface 26 to the host computer side of a striping IDE controller 70. The disk drive side of IDE controller 70 is connected by IDE bus 72 to IDE drive 30 and by IDE bus 74 to a second IDE drive 76. A similar configuration consisting of a second striping IDE controller 78 and IDE drives 82 and 84 may but need not be connected to a second IDE bus 32. Each IDE drive, 30, 76, 82 and 86 contain conventional IDE electronics 36 and a disk assembly 38.

When a system access request is received by the striping controller 70, the request is translated into two requests for two physical drives in an interleaving fashion such that even sectors in the system access request are accessed on one physical disk drive, for example drive 30 and odd sector in the system access request are accessed on disk drive 76. This is accomplished by mapping of the bits in the system request into two physical drive requests.

Referring now to Figure 6, the least significant bit, that is the 0 bit in sector string 42 of system request 40 is mapped to the drive select bit 92 of drive request 90. Bit 1 of sector request 42 is mapped to bit 0 of sector request 94 of drive request 90 and so forth. This leaves the most significant bit (msb), that is bit 5 of sector select string 92, open. This position is taken by the least significant bit (lsb), that is bit 0, of track select string 44 of system request 40. Bit 1 of track select string 44 is mapped to bit 0 of track request string 96 of drive request 90 and so forth. This leaves the msb, that is bit 10 of track select string 96, open. This position is taken by the least significant bit, that is bit 0, of head select string 46 of system request 40. Bit 1 of head select string 46 is mapped to bit 0 of head request string 98 of drive request 90 and so forth. This

leaves the msb, that is bit 3 in the preferred embodiment of head request string 98 open. This position is not filled in the preferred embodiment.

Because a Personal Computer (PC) system has two IDE interfaces at two different input/output (I/O) addresses and each IDE interface can access two disk drives, there are a maximum of eight physical hard disks that can be mapped to four logical disks with the present invention.

Figure 7 illustrates an example of how the mapping set out in Figure 6 creates striping. Referring now to Figure 7, the operating system makes a request for 8 sectors starting with sector 33. The binary address of each sector is set out in table 1 of the example shown in Figure 7. According to the invention, the sector request is shifted right by one bit. This causes the least significant bit to drop out of the address and therefore this bit can be used for something else. In the present invention, this bit is used to select the drive. Thus, in sector 33 where the least significant bit is set to 1, that request would map to drive 1. That is, the 600001 address would drop the last 1 and make a sector request for 60000 which amounts to a request for sector 16 on drive 1. For sector 34, which is binary address 600060, the least significant bit is 0 which is interpreted such that request goes to drive 0. The address is for sector 17 on drive 0. Other addresses are mapped similarly. The next request would be a request for sector 17 from drive 1. The next request would be for sector 18 from drive 0. Then sector 19 from drive 1. etc.

Figure 8 is a schematic of a preferred embodiment of a striping IDE controller according to the present invention. Referring now to Figure 8, striping IDE controller 70 has exclusive OR

("XOR") gate 200 with inputs 202 and 204, both of which are connected to IDE interface 26. Input 202 is connected through interface 26 to the LSB of the current sector address. Input 204 is the least significant bit from the first sector to be transferred. (In an XOR gate, the output is enabled if either of the inputs is enabled but both inputs are not enabled.) The output 206 of XOR 200 is connected to gating input 208 of first-in-first-out ("FIFO") memory 210. Output 206 of XOR 200 is also connected to the input of inverter 212. The output of inverter 212 is connected to gating input 214 of FIFO memory 216. FIFO memories 210 and 216 may be 32kx8 static random access memories (SRAM). Bus 218 includes 16 data lines which carry 16 bits (two bytes) of data in parallel from IDE interface 26 and supplies it simultaneously to data inputs 220 and 222 of FIFO memories 210 and 216. However, gating inputs 208 and 214 operate such that FIFO 210 and 216 memories only receive data when the gating input is activated. The outputs of FIFO memories 210 and 216 are connected to IDE disk drives 30 and 76 respectively by data busses to the respective IDE drive. Figure 8 is a physical implementation of Figure 7. Operationally, Figure 8 translates alternating sector requests to alternating disk drives.

Figure 9 illustrates an example of how virtual sector starting addresses and sector counts are mapped to physical starting addresses and counts. Referring to Figure 9, S_0 and S_1 refer to starting sector addresses. When the address is even, each physical drive (Dr_0 and Dr_1) are provided addresses exactly one-half of the virtual (system) address. When an odd starting address is provided, Dr_0 is provided an address rounded up and Dr_1 is provided an address rounded down.

C_0 and C_1 refer to sector count. When the count is even, both physical drives (Dr_0 and

Dr_1) are provided counts exactly one-half of the virtual (system) count. When the count is odd, Dr_0 is rounded up if the starting address is even; Dr_0 is rounded down for odd starting addresses. Dr_1 is rounded down when Dr_0 is rounded up; Dr_1 is rounded up when Dr_1 is rounded down.

The design of the present invention as described above according to its preferred embodiment achieves the goals of striping (doubling disk throughput B_1 accessing two drives simultaneously) with minimal hardware (most other designs require a microprocessor and or ASIC) and an interface which appears to the operating system as standard IDE interface. Other implementations require custom drivers.

Thus, a low cost, high performance disk drive striping solution is shown. From the above description and drawings, it will be understood by those of ordinary skill in the art that the particular embodiments shown and described are for purposes of illustration only and are not intended to limit the scope of the invention. Those of ordinary skill in the art will recognize that the invention may be embodied in other specific forms without departing from the essence of the invention as defined in the following claims.

CLAIMS

What is claimed is:

1. A striping disk controller for a computer system wherein said computer system includes a CPU connected to a system bus and executes an operating system including a BIOS, said striping disk controller comprising:

an interface connected to said system bus and communicating with said BIOS;

first and second disk drives each having data separator electronics, data formatting electronics and head positioning electronics;

a striping controller connected between said first and second disk drives and said interface, said striping controller adapted to cause data being communicated between said system bus and said first and second drives to be written to and read from said first and second drives in an interleaved form and substantially in parallel.

2. The system of claim 1 wherein said data being communicated between said system bus and said first and second drives is subdivided into a plurality of sequential blocks and said first drive is accessed for every other block of data and said second drive is accessed for the remaining blocks.

3. The system of claim 1 wherein said BIOS supplies a system request that includes a sector bit string, a head bit string, a track bit string and a driver bit and wherein said striping controller maps bits of said system request to a first system request data structure to be

supplied to said first disk drive and a second system request data structure to be supplied to said second disk drive.

4. In a method of writing data onto two disk drives connected to a host computer having an operating system, wherein said operating system generates a system request intended for a single physical drive and wherein said request includes a sector request, a track request and a head request, each said request includes a bit string having a predetermined number of bits, said method including the steps of:

shifting the sector request bit string one bit to the right so that the least significant bit is no longer associated with said sector request; and

using said right shifted least significant bit to select between a first and a second physical drive.

ABSTRACT

The present invention is a striping disk controller used in a computer system that includes a CPU connected to a system bus and running an operating system and having a BIOS. A disk drive interface is connected to the system bus and communicates with the BIOS. First and second disk drives are provided, each including analog electronics, data separator electronics, formatting electronics and head positioning electronics. A striping controller is connected between the first and second disk drives and the interface. The striping controller causes data being communicated between the system bus and the first and second drives to be written and read to and from the first and second dries substantially in parallel, alternating sectors on each drive. Striping increases data transfer rates by accessing two drives simultaneously. During read and write operations, both drives are accessed simultaneously which has the effect of doubling the effective transfer rate and capacity.

FIGURE 1

PRIOR ART

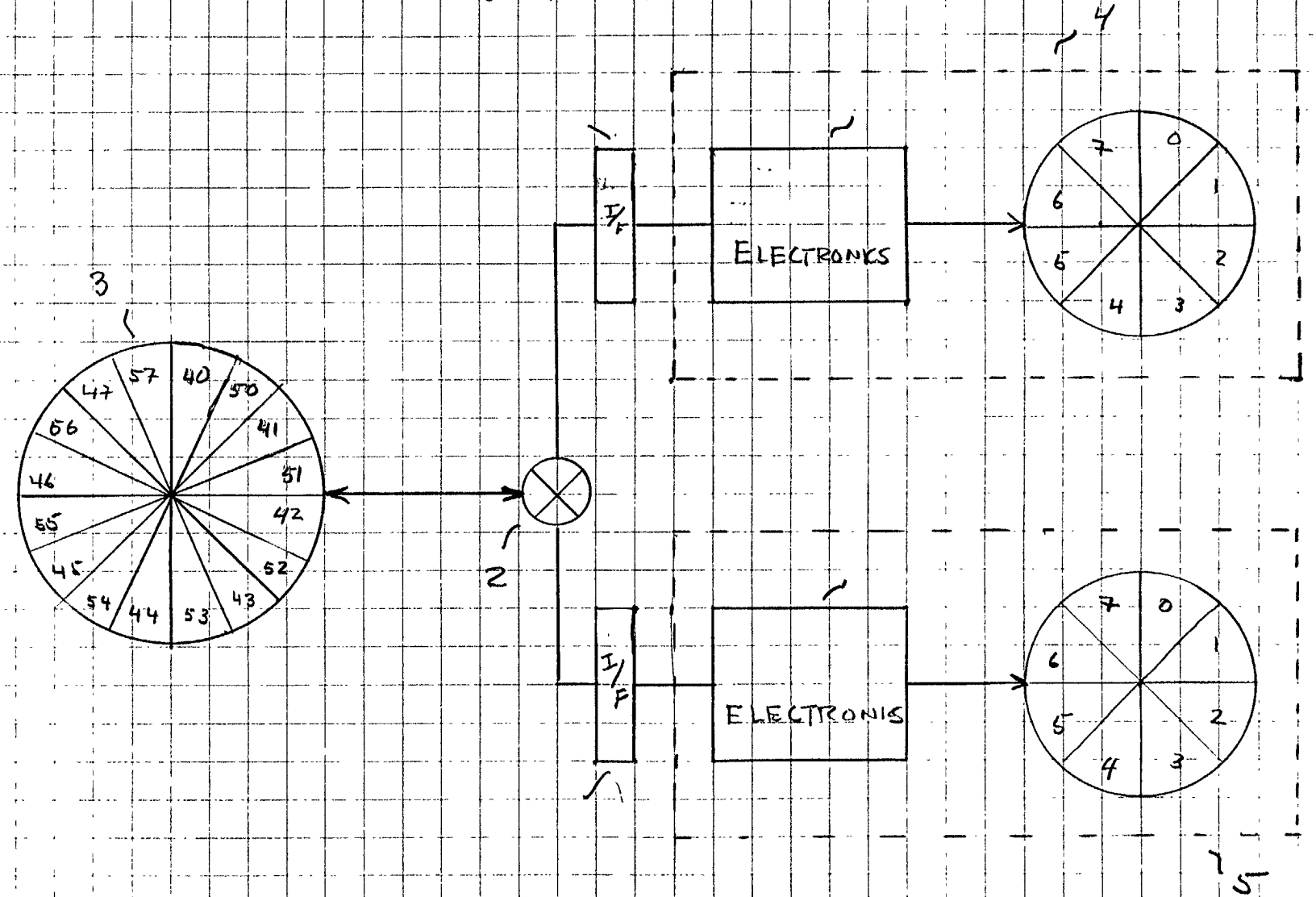


FIG. 2
PRIOR ART

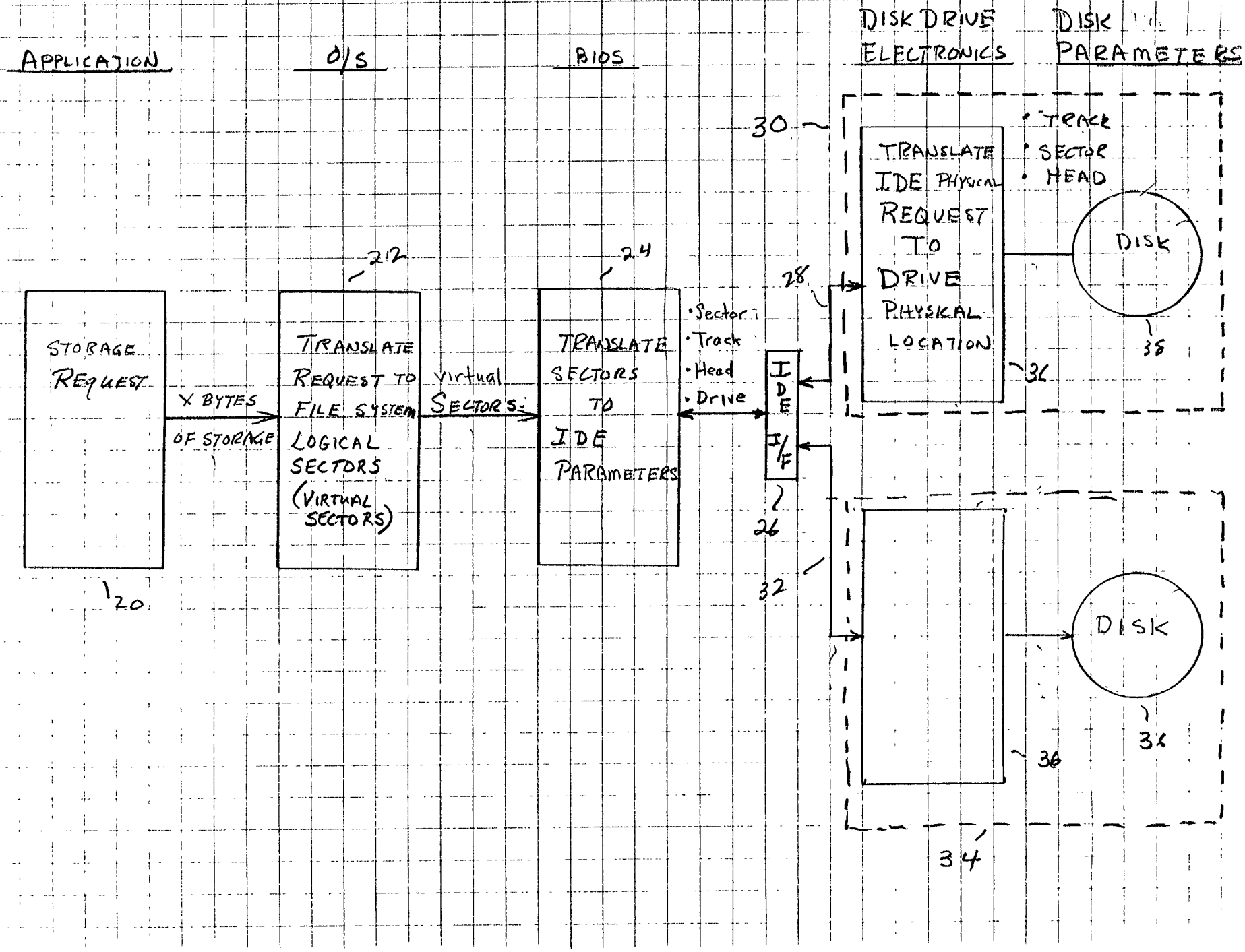


FIG 3

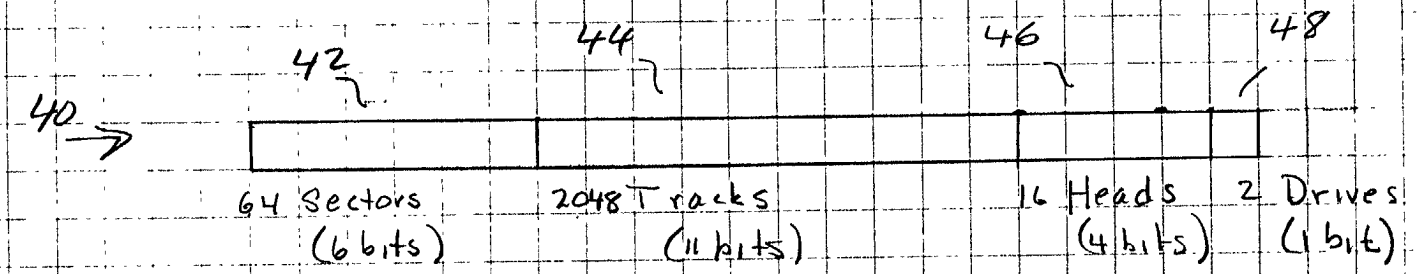

40
42
44
46
48
64 Sectors (6 bits)
2048 Tracks (11 bits)
16 Heads (4 bits)
2 Drives (1 bit)

Figure 4

PRIOR ART

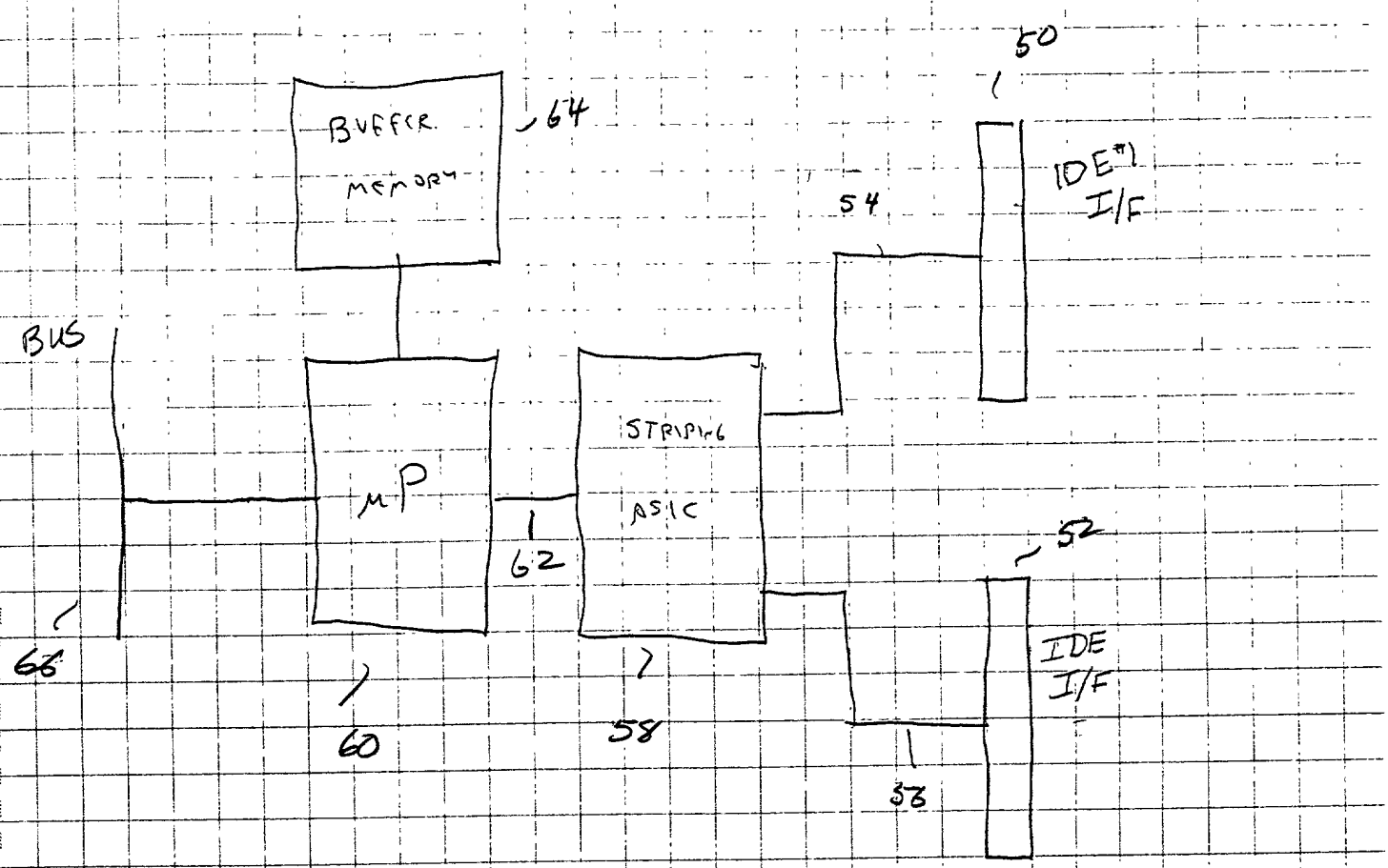


FIGURE 5 Prior Art

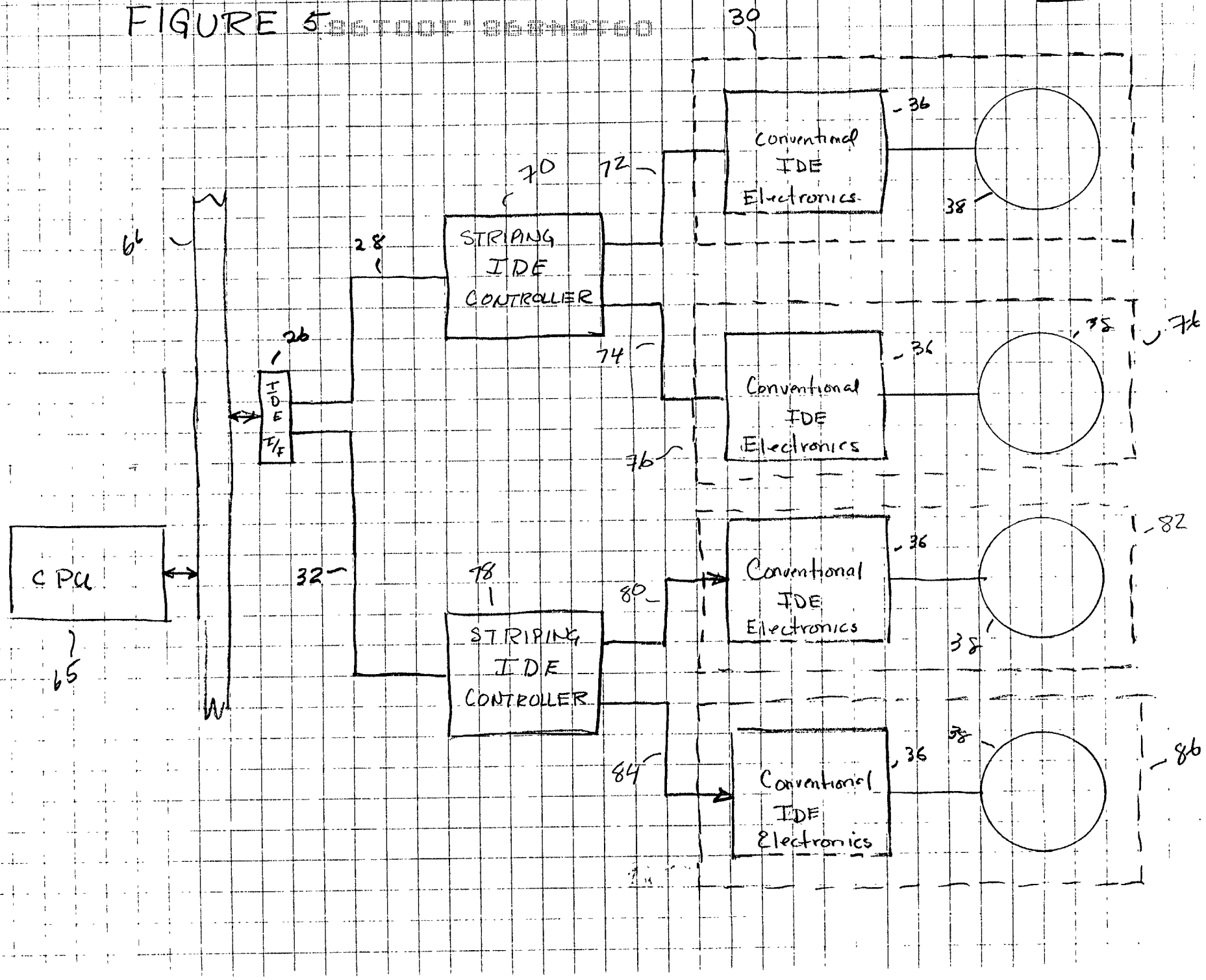
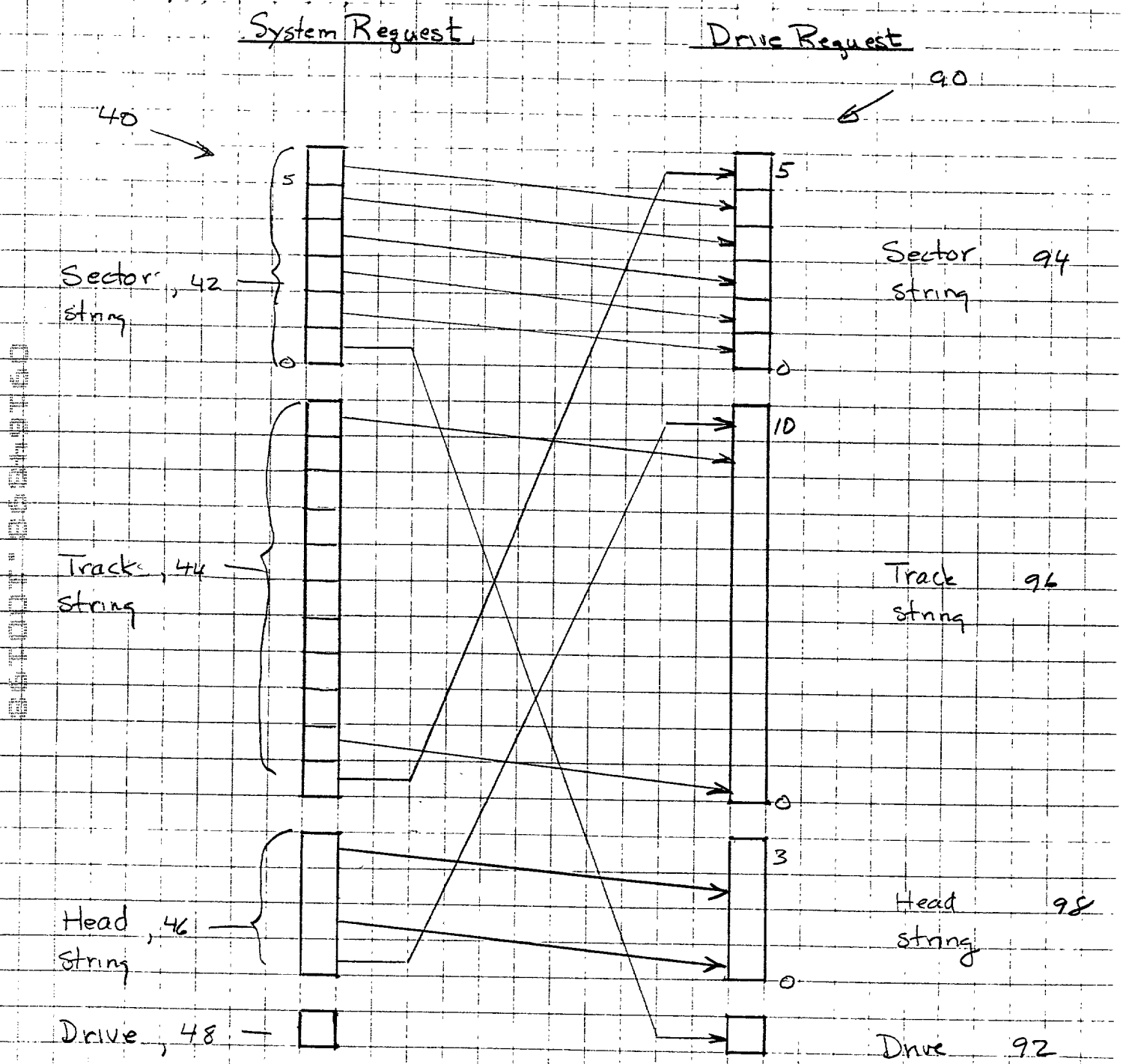


FIGURE 6


System Request
Drive Request
40
90
5
0
Sector, 42
string
Sector
string
94
10
Track, 44
string
Track
string
96
3
Head, 46
string
Head
string
98
Drive, 48
Drive
92

EXAMPLE ONE

Figure 7

THE O/S MAKE A REQUEST FOR 8 SECTORS OF DATA STARTING WITH SECTOR 33. THE SECTORS REQUEST (AND THEIR BITS SET) ARE:

	Sector address
33	100001
34	100010
35	100011
36	100100
37	100101
38	100110
39	100111
40	101000

OUR PROPOSAL SHIFTS THE SECTOR REQUEST RIGHT 1-BIT AND USES THE LSB TO SELECT THE DRIVE

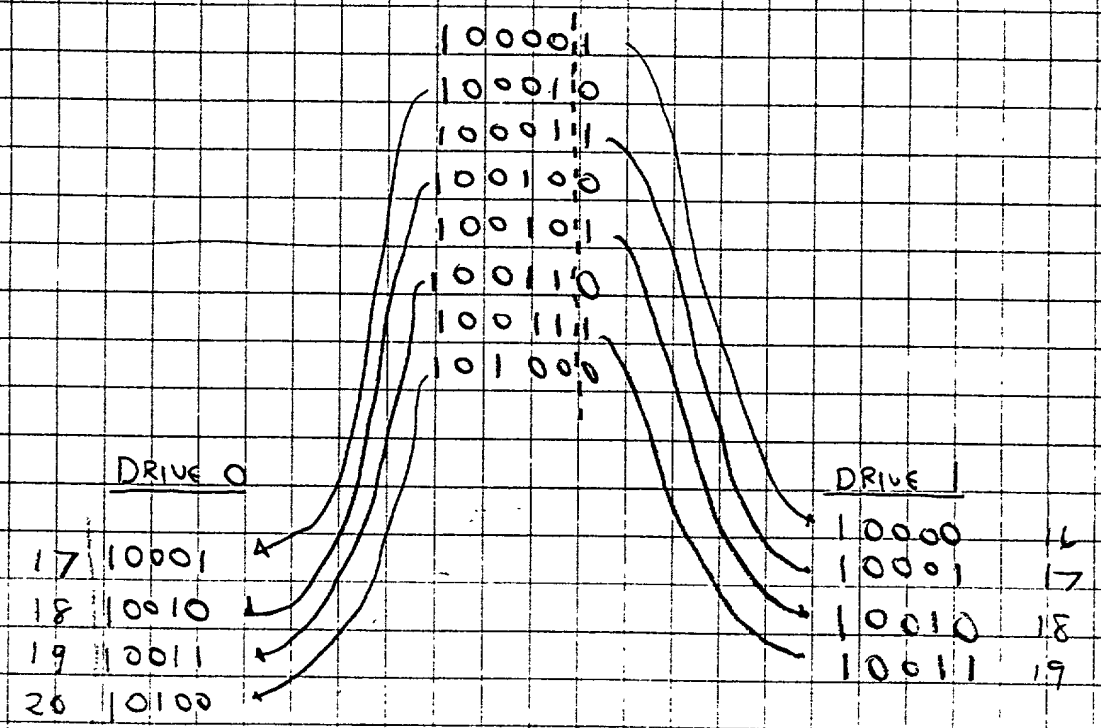


FIGURE 8

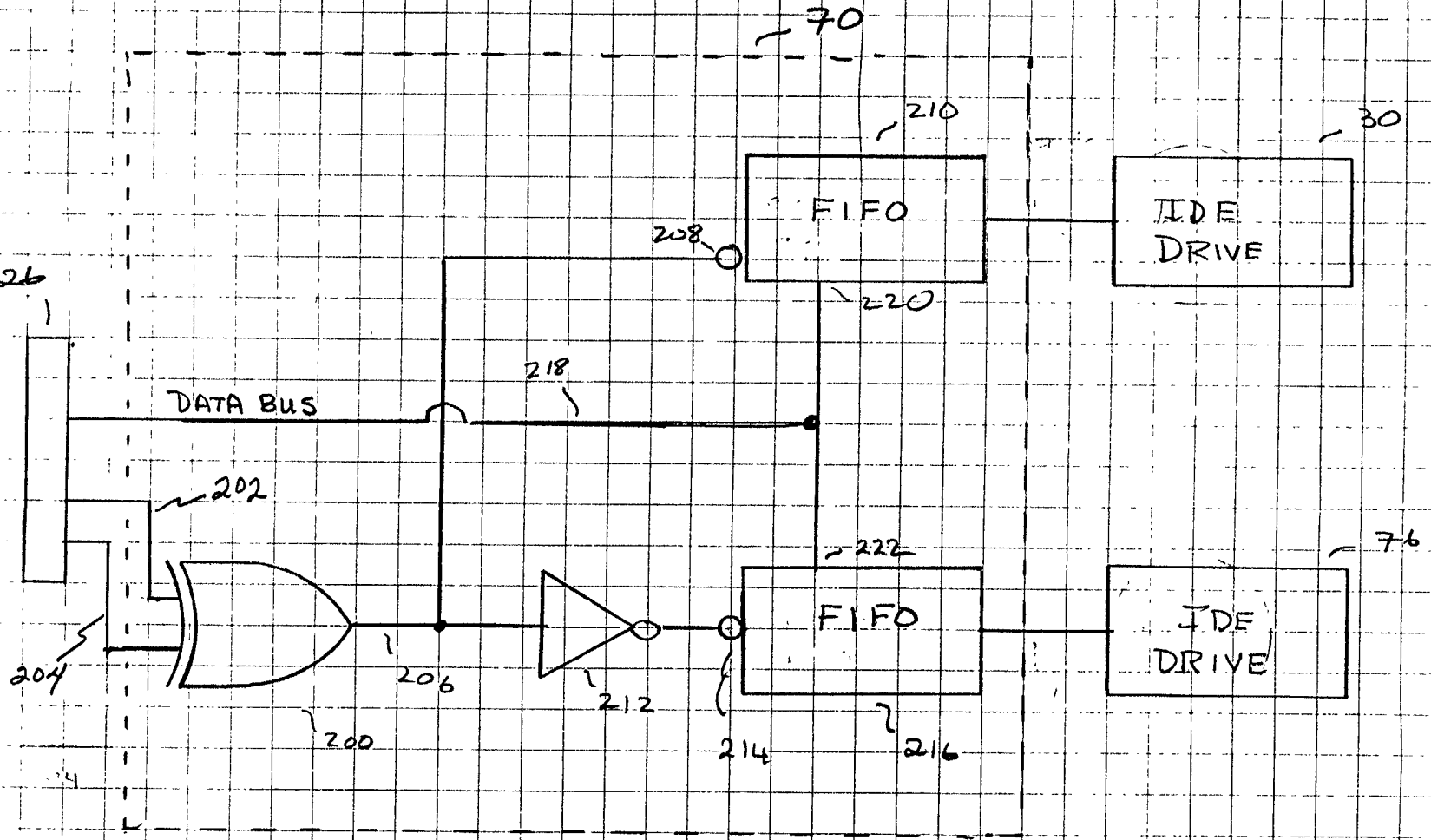

70
210
30
FIFO
IDE DRIVE
208
26
220
218
DATA BUS
202
222
76
FIFO
IDE DRIVE
204
206
212
200
214
216

FIG 9

		Even Count		Odd Count	
		Dr. 0	Dr 1	Dr 0	Dr 1
Even start	Start	0	0	0	0
	Count	0	0	+1	0
Odd start	Start	+1	0	+1	0
	Count	0	0	0	+1

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

VIRTUALIZED STRIPING CONTROLLER

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. P42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, P41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, P42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. P43,021; Babak Redjaian, P42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. P42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. P43,237; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. P42,781;

Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to James H. Salter, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)

ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct

telephone calls to James H. Salter, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor James Akiyama

Inventor's Signature [signature] Date 9/30/98

Residence Beaverton, Oregon (City, State) Citizenship USA (Country)

Post Office Address 15330 SW Heron Court
Beaverton, OR 97007

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.